providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode of operation;

[providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation;

generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation;]

switching modes to a burst mode of operation; and

[providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode of operation]

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation; and

generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on December 15, 1999, and the references cited therewith.

Claims 46 and 61 are amended by this response to clarify the subject matter and to correct typographical errors. No substantive amendment has been made. Instead, words have been rearranged to correct the errors and simply to clarify the claims. Claims 1-9, 33-35, 46, 48-50 and 59-64 remain pending in this application.

With respect to the request of paragraph 3 of the Office Action, Applicant has already updated the information, and will continue to update throughout prosecution if the status of any of the applications or patents changes.

Claims 62-64 were presented as new claims with the Continuing Prosecution Application filed September 30, 1999, which was acknowledged as acceptable in paragraph 1 of the Office Action. As such, no constructive election can properly have been made. If the Office wishes to require an election, that is the choice of the Office. However, no constructive election has been made. Further, Applicant submits that the subject matter of claims 62-64 is consistent with that of the remaining claims.

Claims 59-62 were objected to as not appearing substantially different from claims 1-9, 33-35, 46 and 50. Substantial differences clearly exist in the scope of the claims. Applicant submits that each independent claim has its own different subject matter or scope. Each and every limitation must be considered when determining differences in the claims. Each difference creates different subject matter and scope which significantly varies the scope and subject matter of the claims. Specifically, the claims recite different subject matter. For example, claims 59 and 60 each recite "receiving a burst/pipeline signal" and "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device *in response to the burst/pipeline signal.*" No such elements are found in any of claims 1-9, 33-35, 46 and 50. The scope of the claims is clearly different. Claim 62

§103 Rejection of the Claims

Claims 1-9, 33-35, 46, 48-50, and 59-64 were rejected under 35 USC § 103(a) as being unpatentable over Manning (U.S. Patent No. 5,610,864) in view of Ryan (U.S. Patent No. 5,966,724). Applicant strongly traverses the rejection, and submits that the Office Action fails to state a prima facie case to support the rejection.

A prima facie case under 35 USC § 103 requires that each of the elements of the claim be present in the references, that there be some motivation or suggestion to combine the references, and that there be a reasonable likelihood of success of the combination. The Office Action fails to show motivation or suggestion to combine, and it fails to show each and every element of the claims. As such, the rejection cannot stand. The claims are believed allowable.

Specifically, Applicant continues to dispute that Manning shows a pipelined mode of operation. Ryan discusses only a synchronous burst access memory device, as is clear from a reading of the Ryan disclosure. Within the Ryan synchronous burst memory device, certain addresses can be received in a pipeline method. However, Ryan does not switch between a burst and a pipelined mode of operation. Instead, within a burst operation, pipelined addresses may be received. In fact, Applicant can find no reference in col. 4, ll. 21-26, or for that matter in the entire Ryan specification, of any switching between burst and pipelined modes of operation. Instead, as has been mentioned, the memory device of Ryan is a synchronous burst access memory device.

Applicant further submits that there is no motivation to combine Manning and Ryan. Switching between burst and pipelined modes of operation is not suggested in either Ryan, Manning, or any combination thereof. As has been discussed, no actual switching between burst and pipelines modes of operation is discussed in Ryan. Instead, within a burst mode, pipelined addresses may be received. This is fundamentally different from switching between burst and pipelined modes of operation. As no mention has been made in either reference of switching between burst and pipelined modes of operation, such a combination does not include the switching. Further, combination of the references does not result in both burst and pipelined modes of operation. Instead, as has been mentioned before in earlier arguments, which are incorporated herein again, it is only hindsight gained from Applicant's disclosure which suggests having both burst and pipelined modes of operation in a memory, and switching therebetween.

Manning and Ryan are further not properly combinable as Manning is directed to asynchronous memories and Ryan to synchronous memories. It is a specific unaddressed problem of asynchronous DRAMs to switch between burst and pipelined modes of operation since it was not previously needed. See the background of the invention, page 5, ll. 16-22. Claims 1-9, 46, 48-50 and 59-61 are each directed specifically to an asynchronous memory. Since Ryan is clearly and unambiguously directed to a synchronous memory, Ryan is not properly used in combination with Manning. As such, claims 1-9, 46, 48-50 and 59-61 are believed allowable.

Further, claims 59-60 and 62 each recite "receiving a pipeline/burst select signal" not present in the cited art either alone or in combination. As such, the rejection cannot stand.

Still further, claims 63 and 64 each recite "mode circuitry" which has not been shown to be present in the cited art, either alone or in combination.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 15 March 2000 By Daniel J. Polglaze

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **March 15, 2000**.

DANIEL J. POLGLAZE
Name

Signature